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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,613	07/24/2003	Koji Numazaki	01-449	7912

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POSZ & BETHARDS, PLC
11250 ROGER BACON DRIVE
SUITE 10
RESTON, VA 20190

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,613	NUMAZAKI ET AL	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *2, 6-8 and 10-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,9 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/625613 Attorney's Docket #: 01-449
Filing Date: 7/24/2003; claimed foreign priority to 7/31/2002

Applicant: Numazaki et al.

Examiner: Alexander Williams

Applicant's election without traverse of species of Figures 1A-1D, 2A-2C and 3A-3C (claims 1, 3, 4, 5, 9 and 15), filed 10/21/2004, has been acknowledged.

This application contains claims 2, 5-8 and 10-14 drawn to an invention non-elected without traverse.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, and with respect to claims 1 and 9, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claims 1, 3, 4, 5, 9 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsuzaki et al. (U.S. Patent # 5,264,730).

1. Matsuzaki et al. (figures 1(a) to 7(b)) specifically figures 3(a) and 3(b) show a composite integrated circuit device comprising: a lead frame **2,21**; a substrate **1** whose bottom surface is attached with an adhesive **7** over a top surface of a seat member of the lead frame; a heater element **13** that generates heat while running and is mounted on a first area of the top surface of the substrate; and a temperature-restricted element **11** that has restriction in operating temperature and is mounted on a second area of the top surface of the substrate, wherein the lead frame and the substrate are molded with a mold resin **6**, wherein the seat member of the lead frame includes a hollow member **(the missing portion of 21,2 there between)** that corresponds to a given area of the top surface of the substrate, and wherein the given area includes at least a portion of an intermediate area that is located between the first area and the second area. In regards

to the heated while running and in operating temperature language during the process of the operation of the device, the examiner gives little weigh in examining the claims. The Examiner is interested in finding the final structure claimed in the claims.

3. The composite integrated circuit device according to Claim 1, Matsuzaki et al. show wherein the given area is formed as being surrounding the first area.

4. The composite integrated circuit device according to Claim 3, Matsuzaki et al. show wherein the given area includes the first area.

5. The composite integrated circuit device according to Claim 3, Matsuzaki et al. show wherein the given area is formed as being furthermore surrounding the intermediate area.

9. The composite integrated circuit device according to Claim 1, Matsuzaki et al. show wherein the hollow member is formed through cutting of press work (The examiner is only in the final structure claimed by Applicant).

15. The composite integrated circuit device according to Claim 1, Matsuzaki et al. show wherein the given area is larger than at least one of the first area and the second area.

As to the grounds of rejection under section 103, see MPEP § 2113.

DOCUMENT-IDENTIFIER: US 5264730 A

(11) FIG. 3(a) illustrates a circuit substrate 10 comprising the substrate 1, a semiconductor integrated circuit chip 11 as an active element, and a capacitor 12 and a resistor 13 as passive elements. These active and passive elements are disposed on and fixed to the substrate 1. Electrical connections between a terminal of these elements and a printed circuit pattern (not shown)on the substrate 1 are made by a bonding wire 5 or by direct soldering. The circuit substrate 10 is disposed on four stages 21 of the lead frame 2. Each terminal of the inner lead 24b is connected to a bonding pad (not shown) on the substrate 1 by a bonding wire 5.

(12)In this embodiment, the substrate 1 is made of ceramic and has a thickness of 0.6 mm and a surface area of 23.times.23 mm. On each side of the square shape of the substrate 1, a plurality of devoid portions 3a are formed at regular intervals of 1.6 mm between adjacent devoid portions, each having a shape of a semicircle of 0.4 mm in diameter. The length of the intervals can vary from the 1.6 mm in this embodiment. The shape of all or some of the devoid portion can be semicircular, elliptical, V-shaped, U-shaped or the like.

Notch-like devoid portions 3a, as illustrated, are formed on the periphery of the ceramic substrate 1 and can be any of the

above-mentioned shapes. The notch-like devoid portions formed on the periphery result in elongation of the actual length of the periphery (edge) contacting with the mold package and result in increased strength after packing of the adhesion force between the substrate 1 and the mold 6.
13) As shown in FIG. 3(a), the substrate 1 of the embodiment further includes a plurality of devoid portions 3b of a through-hole type. These through-holes have a diameter of 0.2 mm and are spaced a regular intervals of 1.6 mm arranged along a line spaced 2 mm from each side of the square.
(14) In the above embodiment, both the lead frame 2 and the entire circuit substrate 10 are encapsulated by a transfer-mold process using a thermosetting resin such as an epoxy resin. After molding, the outer leads 24a are shaped and unnecessary portions cut off, thereby completing fabrication of a hybrid integrated circuit of a PQFP (Plastic Quad-Flat Package) type having outside dimensions of 28.times.28.times.4 mm.
(15) FIG. 3(b) is a schematic cross section of the hybrid integrated circuit after mold packaging taken along a line X--X'. Though the stages 21 are not positioned on the line X--X', the stage 21 is illustrated in FIG. 3(b) for easy understanding, and it is clear that the stage 21 is lowered from the level of the inner lead 24b.
(16) To summarize the above embodiment, the devoid portions are formed along the periphery and along a line spaced from each side of a square substrate, and four stages are utilized as a support. This embodiment of the hybrid integrated circuit will hereinafter, for convenience, be designated test piece group 1.

Claims 1, 3, 4, 5, 9 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirakawa et al. (U.S. Patent # 6,484,708 B2).

1. Hirakawa et al. (figures 1 to 8) specifically figures 1 and 4 show a composite integrated circuit device comprising: a lead frame **6,3**; a substrate **4** whose bottom surface is attached with an adhesive **2** over a top surface of a seat member of the lead frame; a heater element **(the resistor, see column 3, lines 31-37)** that generates heat while running and is mounted on a first area of the top surface of the substrate; and a temperature-restricted element **(the MIC, see column 3, lines 31-37)** that has restriction in operating temperature and is mounted on a second area of the top surface of the substrate, wherein the lead frame and the substrate are molded with a mold resin

7, wherein the seat member of the lead frame includes a hollow member **3b** that corresponds to a given area of the top surface of the substrate, and wherein the given area includes at least a portion of an intermediate area that is located between the first area and the second area. In regards to the heated while running and in operating temperature language during the process of the operation of the device, the examiner gives little weigh in examining the claims. The Examiner is interested in finding the final structure claimed in the claims.

3. The composite integrated circuit device according to Claim 1, Hirakawa et al. show wherein the given area is formed as being surrounding the first area.

4. The composite integrated circuit device according to Claim 3, Hirakawa et al. show wherein the given area includes the first area.

5. The composite integrated circuit device according to Claim 3, Hirakawa et al. show wherein the given area is formed as being furthermore surrounding the intermediate area.

9. The composite integrated circuit device according to Claim 1, Hirakawa et al. show wherein the hollow member is formed through cutting of press work (The examiner is only in the final structure claimed by Applicant).

15. The composite integrated circuit device according to Claim 1, Hirakawa et al. show wherein the given area is larger than at least one of the first area and the second area.

As to the grounds of rejection under section 103, see MPEP § 2113.

The listed references are cited as of interest to this application, but not applied at this time.

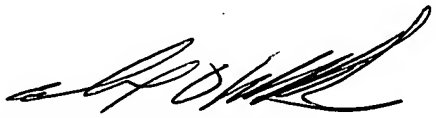
Field of Search	Date
U.S. Class and subclass: 257/787,676,783,666,685,686,777,702,703,680,773,774,723,528,533,534,537,712,713,705,717,720,675,724,725,728 361/705,719,704,748	1/9/05
Other Documentation: foreign patents and literature in 257/787,676,783,666,685,686,777,702,703,680,773,774,723,528,533,534,537,712,713,705,717,720,675,724,725,728 361/705,719,704,748	1/9/05

Electronic data base(s): U.S. Patents	1/9/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Alexander O Williams
Primary Examiner
Art Unit 2826

1/9/05
AOW